REMARKS

Claims 1-61 are pending in this application with claims 1, 11, 21, 33, 46, 50 and 54 being independent. Claim 1 has been amended.

Applicant acknowledges with appreciation the Examiner's allowance of claims 11-20 and 46-58, and the Examiner's indication that claim 61 is directed to allowable subject matter.

Independent claim 1 and its dependent claims 2, 4, 9 and 10 have been rejected as being unpatentable over Okumura (U.S. Patent No. 5,945,972) in view of Perner (U.S. Patent No. 6,115,019).

Claim 1 has been amended to recite "a write-in transistor electrically connected to the selected one of the plurality of storage circuits *through the write-in storage circuit selection portion*" (emphasis added) and "a read transistor electrically connected to the selected one of the plurality of storage circuits *through the read storage circuit selection portion*" (emphasis added). Applicants request reconsideration and withdrawal of the rejection of claim 1 and its dependent claims 2, 4, 9, and 10 because neither Okumura, Perner, nor any combination of the two describes or suggests the recited write-in transistor or the recited read transistor.

Okumura describes a display device having a memory circuit configuration that reduces power dissipation. As the Examiner admits on p. 3 of the Office Action, Okumura does not describe or suggest a write-in transistor electrically connected to the write-in storage circuit selection portion, much less a write-in transistor electrically connected to one of the storage circuits through the write-in storage circuit selection portion. Similarly, as the Examiner also admits on p. 3 of the Office Action, Okumura does not describe or suggest a read transistor electrically connected to the read storage circuit selection portion, much less a read transistor electrically connected to one of the storage circuits through the read storage circuit selection portion.

Perner describes a liquid crystal display device having pixels with storage elements that relax the data rate and bandwidth requirements typically imposed by operation of a LCD device. In Perner, the transistor 32, which the Examiner equates to the recited write-in transistor, is not electrically connected to the storage transistor 34 through the write word line 14, which the

Examiner equates to the recited write-in storage circuit selection portion. Rather, the transistor 32 is directly connected to the storage transistor 34. Accordingly, Perner does not describe or suggest a write-in transistor "electrically connected to selected one of the plurality of the storage circuits *through the write-in storage circuit selection portion*" (emphasis added), as claimed.

Similarly, the transistor 36 or 38, which the Examiner equates to the recited read transistor, is not electrically connected the storage transistor 34 through the read line 18 or 22, which the Examiner equates to the recited read storage circuit selection portion. Rather, the transistor 36 is directly connected to the storage transistor 34, and the transistor 38 is connected to the storage transistor 34 through the transistor 36. Accordingly, Perner does not describe or suggest a read transistor "electrically connected to selected one of the plurality of the storage circuits *through the read storage circuit selection portion*" (emphasis added), as claimed.

For at least these reasons, applicants request reconsideration and withdrawal of the rejection of claim 1 and its dependent claims 2, 4, 9, and 10.

Claim 3 has been rejected as being unpatentable over Okumura in view of Perner and Yamazaki (U.S. Patent No. 5,349,366); claims 5 and 6 have been rejected as being unpatentable over Okumura in view of Perner and Fonash (U.S. Patent No. 5,945,866); claim 7 has been rejected as being unpatentable over Okumura in view of Perner and Johnson (U.S. Patent No. 4,752,118); and claim 8 has been rejected as being unpatentable over Okumura in view of Perner and Kobayashi (U.S. Patent No. 4,432,610). Applicant requests reconsideration and withdrawal of this rejection because neither, Yamazaki, Fonash, Johnson, nor Kobayashi remedies the failure of Okumura and Perner to describe or suggest the subject matter of claim 1.

With respect to the provisional double patenting rejection of claims 21-45 and 59-60 over claims 3-5 and 8-13 of Application No. 09/912,596, applicant request that this rejection be held in abeyance until the claims of both of these applications are otherwise found to be allowable. Applicants note that Application No. 09/912,596 has not been passed to issue because a Request for Continued Examination was filed on February 17, 2005.

Enclosed is a $120 check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 5/25/05

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